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PATENT APPLICATION  
10/825,021

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Shannon V. Davidson et al.  
Serial No.: 10/825,021  
Filing Date: April 15, 2004  
Title: System and Method for Topology-Aware Job Scheduling and Backfilling in an HPC Environment

**Mail Stop: Amendments**  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
Dear Sir:

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*Willie Jiles*  
Willie Jiles

Date: March 8, 2006

### **INFORMATION DISCLOSURE STATEMENT**

Applicants respectfully request, under 37 C.F.R. §§ 1.56, 1.97 and 1.98, that the references listed on the attached PTO-1449 form be considered and cited in the examination of the above-identified patent application. The present Application was filed after June 30, 2003. Therefore, under the July 11, 2003, waiver of 37 C.F.R. § 1.98(a)(2)(i) by the U.S. Patent and Trademark Office, copies of U.S. Patents and U.S. Patent Application Publications listed in the attached PTO-1449 form are not enclosed. All other references are enclosed for the convenience of the Examiner.

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**REMARKS**

Each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than thirty days prior to the filing of this Information Disclosure Statement, and this Information Disclosure Statement is submitted before a first Office Action on the merits. Under 37 C.F.R. § 1.97(b)(3), no fee is due. Nonetheless, the Commissioner is hereby authorized to charge any fee and credit any overpayment to Deposit Account No. 02-0384 of Baker Botts L.L.P.

Respectfully submitted,  
BAKER BOTTS L.L.P.  
Attorneys for Applicants

A handwritten signature in black ink, appearing to read 'T. W. Thomas', with a stylized flourish at the end.

Travis W. Thomas  
Reg. No. 48,667

Date: March 8, 2006

Correspondence Address:

**Customer Number 45507**

PTO-1449		Application No. 10/825,021		Applicant(s) Shannon V. Davidson et al.																																																																
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		<p align="center"><b>U.S. PATENT DOCUMENTS</b></p> <table border="1"> <thead> <tr> <th></th> <th>DOCUMENT NO.</th> <th>DATE</th> <th>NAME</th> <th>CLASS</th> <th>SUBCLASS</th> <th>FILING DATE</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>5,301,104</td> <td>04/05/1994</td> <td>Yalamanchili</td> <td>395</td> <td>800</td> <td>08/07/1990</td> </tr> <tr> <td>B</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> </tbody> </table> <p align="center"><b>FOREIGN PATENT DOCUMENTS</b></p> <table border="1"> <thead> <tr> <th rowspan="2"></th> <th rowspan="2">DOCUMENT NO.</th> <th rowspan="2">DATE</th> <th rowspan="2">COUNTRY</th> <th rowspan="2">CLASS</th> <th rowspan="2">SUBCLASS</th> <th colspan="2">TRANSLATION</th> </tr> <tr> <th>YES</th> <th>NO</th> </tr> </thead> <tbody> <tr> <td>C</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>D</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> </tbody> </table> <p align="center"><b>NON-PATENT DOCUMENTS</b></p> <table border="1"> <thead> <tr> <th></th> <th>DOCUMENT (Including Author, Title, Source, and Pertinent Pages)</th> <th>DATE</th> </tr> </thead> <tbody> <tr> <td>E</td> <td>Communication from the European Patent Office, European Search Report for Application No. PCT/US2005/012314, 6 pages, 09/20/2005, and Written Opinion of the International Search Authority, 7 pages</td> <td>Mailed 02/10/2006</td> </tr> <tr> <td>F</td> <td>Feitelson, "Job Scheduling in Multiprogrammed Parallel Systems", IBM Research Report, August 1997, pages 1-4, XP002942107</td> <td>August 1997</td> </tr> <tr> <td>G</td> <td>Kandlur et al., "Hypercube Management in the Presence of Node Failures", third conference on hypercube concurrent computers and applications ACM New York, 1988, pages 328-336, vol. 1, XP002364194</td> <td>1998</td> </tr> <tr> <td>H</td> <td>Wenjian et al., "Efficient Processor Allocation for 3D Tori", Parallel Processing Symposium 1995, Proceedings, 9th International, April 25-28, 1995, IEEE Comput. Soc., pages 466-471, XP010135921</td> <td>1995</td> </tr> <tr> <td>I</td> <td>Ma et al., "E-Kernel: An Embedding Kernel on the IBM Victor V256, Multiprocessor for Program Mapping and Network Reconfiguration, IEEE Transactions on Parallel and Distributed Systems, IEEE Service Center, vol. 5, no. 9, September 1, 1994, pages 977-994, XP000460490</td> <td>September 1, 1994</td> </tr> </tbody> </table>					DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE	A	5,301,104	04/05/1994	Yalamanchili	395	800	08/07/1990	B								DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION		YES	NO	C								D									DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE	E	Communication from the European Patent Office, European Search Report for Application No. PCT/US2005/012314, 6 pages, 09/20/2005, and Written Opinion of the International Search Authority, 7 pages	Mailed 02/10/2006	F	Feitelson, "Job Scheduling in Multiprogrammed Parallel Systems", IBM Research Report, August 1997, pages 1-4, XP002942107	August 1997	G	Kandlur et al., "Hypercube Management in the Presence of Node Failures", third conference on hypercube concurrent computers and applications ACM New York, 1988, pages 328-336, vol. 1, XP002364194	1998	H	Wenjian et al., "Efficient Processor Allocation for 3D Tori", Parallel Processing Symposium 1995, Proceedings, 9th International, April 25-28, 1995, IEEE Comput. Soc., pages 466-471, XP010135921	1995	I
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